at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

at least one buffer pad attached to the chip and made of a material having a similar thermal expansion coefficient to the chip;

a heat sink having a first surface, a second surface opposed to the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface of the heat sink is attached to the buffer pad for interposing the buffer pad between the heat sink and the chip so as to space the first surface apart from the chip;

an interface layer formed on the second surface of the heat sink, and made of a material having adhesion with a molding compound smaller than adhesion between the heat sink and the molding compound, wherein the interface layer covers the entire second surface of the heat sink; and

an encapsulant made of the molding compound for encapsulating the chip, the buffer pad, the heat sink and the chip carrier, wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant, and the side surfaces of the heat sink are flush with side edges of the encapsulant;

whereby due to relatively smaller adhesion between the interface layer and the molding compound for making the encapsulant, the molding compound remaining on the interface layer during formation of the encapsulant can be removed easily from the interface layer, so as to make the semiconductor package free of flash of the molding compound.

14. (Amended) The semiconductor package of claim 12, wherein the material for making the interface layer on the second surface of the heat sink is selected from the group consisting of gold, chromium, nickel, alloy thereof and Teflon (polytetrafluoroethylene).

REMARKS

Claims 1-20 are pending in the application. Claims 1, 3, 10, 12, and 14 have been amended by the present amendment. The amendments are fully supported by the specification as originally filed (see, e.g., page 9, first paragraph).

Applicants claim a semiconductor package, including: a chip carrier; at least one chip mounted on the chip carrier; a heat sink having a first surface and a second surface opposed to the first surface; an interface layer formed on the second surface of the heat sink and made of a material having adhesion with a molding compound smaller than adhesion between the heat sink and the molding compound, wherein the interface layer covers the entire second surface of the heat sink; and an encapsulant made of the molding compound for encapsulating the chip; wherein due to the relatively smaller adhesion between the interface layer and the molding compound, the remaining molding compound can be removed easily from the interface layer, so as to make the semiconductor package free of resin flash caused by the molding compound.

FIG. 2(H) illustrates the semiconductor package after encapsulation with a molding compound (reference numerals 24 and 240A). Because adhesion between interface layer 233 and molding compound 240A is smaller than adhesion between heat sink 23 and molding compound 24, the molding compound 240A left on the interface layer 233 can be easily removed, without leaving resin flash on the interface layer 233, such that the resulting semiconductor package is free of resin flash (see FIG. 1), thus improving the heat-dissipating efficiency of the semiconductor package. Moreover, the interface layer covers the entire second surface of the heat sink, in order to prevent resin flash on the entire surface of the heat sink.

Claims 1-20 were rejected under 35 USC 112, second paragraph, as being indefinite because of certain language in claims 1 and 12 describing the interaction between the interface layer, molding compound, and heat sink. Claims 1 and 12 have been amended to clarify that the interface layer is made of a material having adhesion with a molding compound that is smaller than adhesion between the heat sink and the molding compound. As described in the specification (see page 9, first paragraph), the term "molding compound" encompasses reference numerals 24 and 240A (see FIG. 2(H)). After encapsulation of the interface layer and heat sink, the result is a semiconductor package in which adhesion between the interface layer/molding compound is smaller than adhesion between the heat sink/molding compound, thereby enabling

easy removal of the molding compound from the interface layer to eliminate resin flash, while ensuring that the molding compound remains adhered to the first surface of the heat sink.

Claims 1, 2, 4, 6, 9, and 10 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,288,900 to Johnson et al. (hereinafter "Johnson"). Claims 3 and 11 were rejected under 35 USC 103(a) as being unpatentable over Johnson in view of U.S. Patent 6,323,065 to Karnezos. Claim 5 was rejected under 35 USC 103(a) as being unpatentable over Johnson in view of U.S. Patent 6,127,724 to DiStefano. Claims 7 and 8 were rejected under 35 USC 103(a) as being unpatentable over Johnson in view of U.S. Patent 6,198,171 to Huang et al. Claims 12, 13, 15, 16, 19, and 20 were rejected under 35 USC 103(a) as being unpatentable over Johnson in view of U.S. Patent 6,236,568 to Lai et al. Claims 14 was rejected under 35 USC 103(a) as being unpatentable over Johnson in view of Lai et al., and further in view of Karnezos. Claims 17 and 18 were rejected under 35 USC 103(a) as being unpatentable over Johnson in view of Lai et al., and further in view of Huang et al. These rejections are respectfully traversed, and for convenience are addressed together.

Johnson discloses a ball grid array (BGA) package structure, including various embodiments of a heat spreading cap, as shown in FIGS. 2-17. The heat spreading cap is shaped or sized to provide distinct combinations of coefficient of thermal expansion (CTE) and stiffness in different regions of the package structure (see column 3, lines 21-25), so as to reduce warpage or bending to thereby reduce overall stress in the package structure. In FIGS. 15 and 16 of Johnson, as cited in the Office Action, the heat spreading cap 22 is composed of layers 40 and 41 having different CTEs or stiffnesses (see column 4, line 64 to column 5, line 9) so as to reduce warpage or thermal stress. Also, the layer 41 does not cover the entire surface of the layer 40.

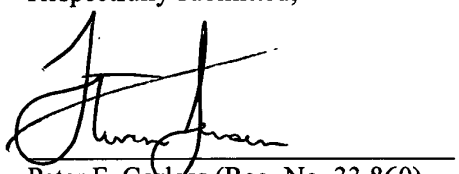
Johnson does not address the problem of resin flash on an interface layer attached to a heat sink, or provide for smaller adhesion between an interface layer/molding compound as compared to adhesion between the heat sink/molding compound. Even if the heat spreading cap 22 in Johnson were somehow considered an "interface layer," it does not extend over the entire surface of a heat sink, as required in the Applicants' claimed invention. Moreover, there is no

teaching or suggestion for providing adhesion between the heat spreading cap 22 and molding compound 24 which is smaller than adhesion between layer 40 and the molding compound.

Claim 12 of the Applicants' invention differs from claim 1 only by interposing a buffer pad between the heat sink and chip. Since Johnson fails to teach or suggest the above-described features of the Applicants' claimed invention, it would not be possible to combine the buffer pad of Lai et al. with Johnson to somehow produce the invention recited in claim 12.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



Date: October 15, 2002

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BOS2_315822.1

APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1, 3, 10, 12, and 14 have been amended as follows:

1. (Amended) A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

a heat sink having a first surface, a second surface [opposing] opposed to the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface of the heat sink is attached to the chip for interposing the chip between the chip carrier and the heat sink;

an interface layer formed on the second surface of the heat sink, [wherein] and made of a material having adhesion [between the interface layer and] with a molding compound [is] smaller than adhesion between the heat sink and the molding compound, wherein the interface layer covers the entire second surface of the heat sink; and

an encapsulant made of the molding compound for encapsulating the chip, [and filling a gap between the first surface of] the heat sink and the chip carrier, wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant, and the side surfaces of the heat sink are [in a coplane] flush with side edges of the encapsulant;

whereby due to relatively smaller adhesion between the interface layer and the molding compound for making the encapsulant, the molding compound remaining on the interface layer during formation of the encapsulant can be removed easily from the interface layer, so as to make the semiconductor package free of flash of the molding compound.

3. (Amended) The semiconductor package of claim 1, wherein the material for making the interface layer on the second surface of the heat sink is [made of a material] selected from [a] the group consisting of gold, chromium, nickel, alloy thereof [or] and Teflon (polytetrafluoroethylene).

10. (Amended) The semiconductor package of claim 1, wherein at a position on the first surface of the heat sink corresponding to the chip there is formed a connecting portion extending toward the chip for connecting the heat sink to the chip through the connecting portion, [while] and the first surface of the heat sink other than the position of the connecting portion [being] is spaced apart from the chip.

12. (Amended) A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

at least one buffer pad attached to the chip and made of a material having a similar thermal expansion coefficient to the chip;

a heat sink having a first surface, a second surface [opposing] opposed to the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface of the heat sink is attached to the buffer pad for interposing the buffer pad between the heat sink and the chip so as to space the first surface apart from the chip;

an interface layer formed on the second surface of the heat sink, [wherein] and made of a material having adhesion [between the interface layer and] with a molding compound [is] smaller than adhesion between the heat sink and the molding compound, wherein the interface layer covers the entire second surface of the heat sink; and

an encapsulant made of the molding compound for encapsulating the chip, [and] the buffer pad, [and for filling a gap between the first surface of] the heat sink and the chip carrier, wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant, and the side surfaces of the heat sink are [in a coplane] flush with side edges of the encapsulant;

whereby due to relatively smaller adhesion between the interface layer and the molding compound for making the encapsulant, the molding compound remaining on the interface layer during formation of the encapsulant can be removed easily from the interface layer, so as to make the semiconductor package free of flash of the molding compound.

14. (Amended) The semiconductor package of claim 12, wherein the material for making the interface layer on the second surface of the heat sink is [made of a material] selected from [a] the group consisting of gold, chromium, nickel, alloy thereof [or] and Teflon (polytetrafluoroethylene).